



CSD13381F4, 12 V N-Channel FemtoFET™ MOSFET

1 Features

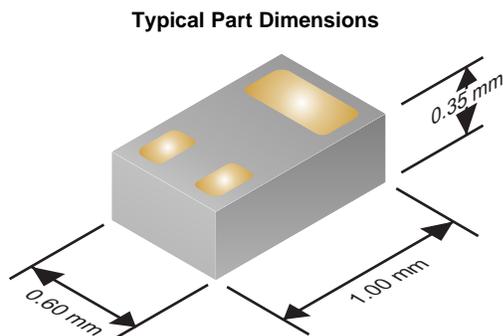
- Low On Resistance
- Low Q_g and Q_{gd}
- Low Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm x 0.6 mm
- Ultra-Low Profile
 - 0.35 mm Height
- Integrated ESD Protection Diode
 - Rated > 4 kV HBM
 - Rated > 2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- Handheld and Mobile Applications

3 Description

The FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Product Summary

V_{DS}	Drain-to-Source Voltage	12	V
Q_g	Gate Charge Total (4.5V)	1060	pC
Q_{gd}	Gate Charge Gate to Drain	140	pC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 1.8V$	310
		$V_{GS} = 2.5V$	170
		$V_{GS} = 4.5V$	140
$V_{GS(th)}$	Threshold Voltage	0.85	V

Ordering Information

Device	Qty	Media	Package	Ship
CSD13381F4	3000	7-Inch Reel	Femto (0402) 1.0 mm x 0.6 mm SMD Lead Less	Tape and Reel
CSD13381F4T	250	7-Inch Reel		

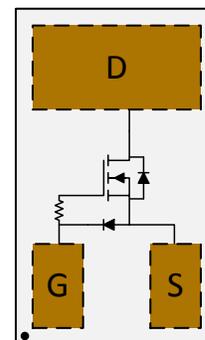
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	8	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	2.1	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	7	A
I_G	Continuous Gate Clamp Current	35	mA
	Pulsed Gate Clamp Current ⁽²⁾	350	
P_D	Power Dissipation ⁽¹⁾	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 7.4\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	2.7	mJ

(1) Typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

Top View





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4 Specifications

4.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	12			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			100	nA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 4\text{ V}$			50	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.65	0.85	1.10	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.5\text{ A}$		310	400	m Ω
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.5\text{ A}$		170	225	m Ω
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.5\text{ A}$		140	180	m Ω
g_{fs}	Transconductance	$V_{DS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$		3.2		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V},$ $f = 1\text{ MHz}$		155	200	pF
C_{oss}	Output Capacitance			47	62	pF
C_{rss}	Reverse Transfer Capacitance			2.5	3.3	pF
R_G	Series Gate Resistance			23		Ω
Q_g	Gate Charge Total (4.5 V)	$V_{DS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$		1060	1400	pC
Q_{gd}	Gate Charge Gate to Drain			140		pC
Q_{gs}	Gate Charge Gate to Source			230		pC
$Q_{g(th)}$	Gate Charge at V_{th}			155		pC
Q_{oss}	Output Charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		1120		pC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 0\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 0.5\text{ A}, R_G = 2\ \Omega$		3.7		ns
t_r	Rise Time			1.5		ns
$t_{d(off)}$	Turn Off Delay Time			11.0		ns
t_f	Fall Time			3.8		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 0.5\text{ A}, V_{GS} = 0\text{ V}$		0.73	0.9	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 6\text{ V}, I_F = 0.5\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		1550		pC
t_{rr}	Reverse Recovery Time			6		ns

4.2 Thermal Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

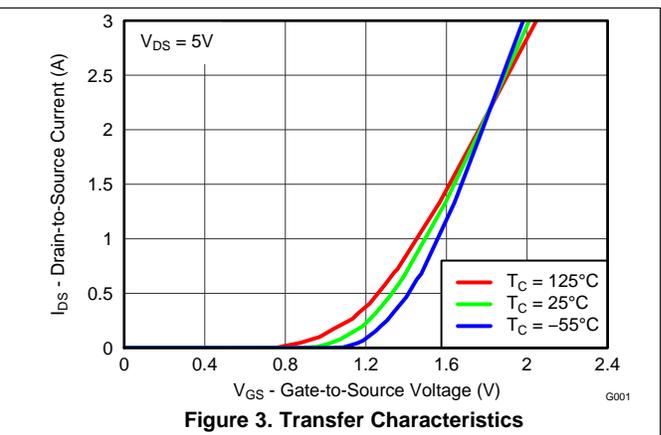
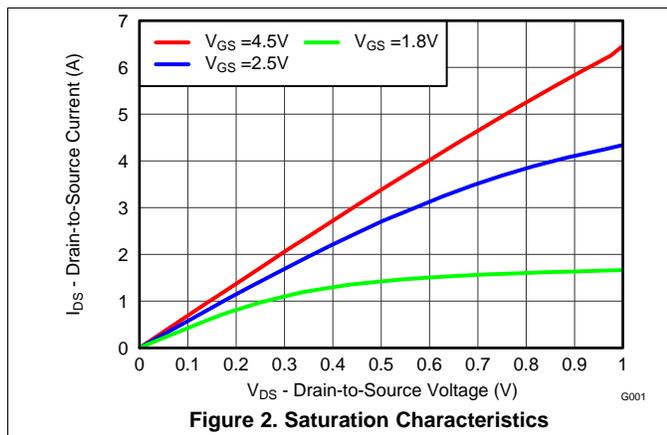
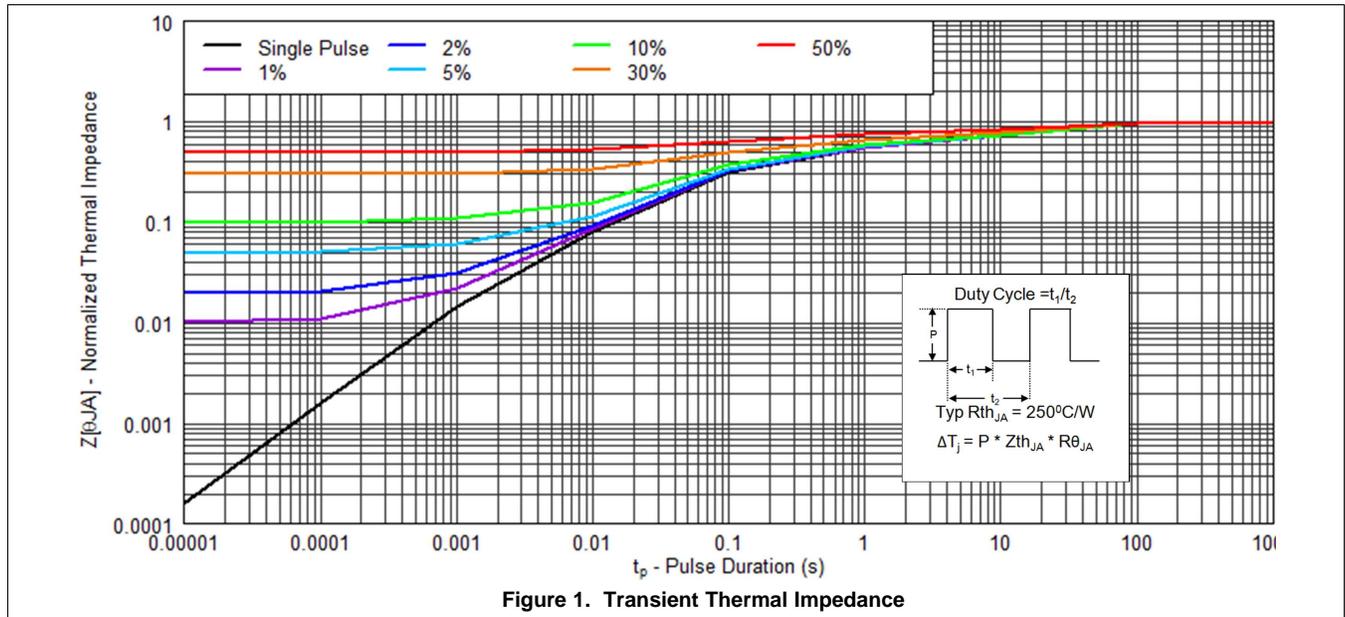
PARAMETER		Typical Values	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾	90	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ⁽²⁾	250	$^\circ\text{C}/\text{W}$

(1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

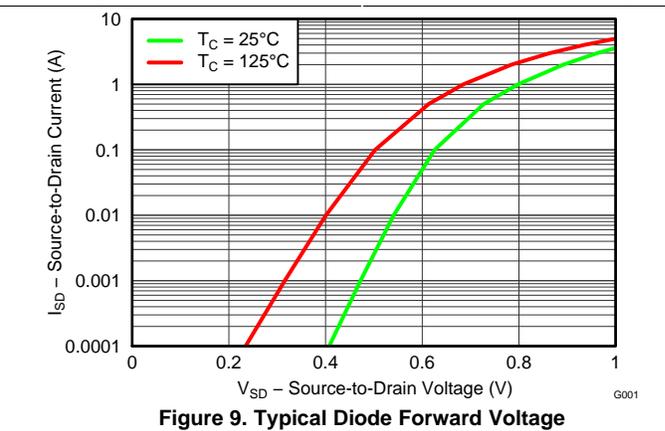
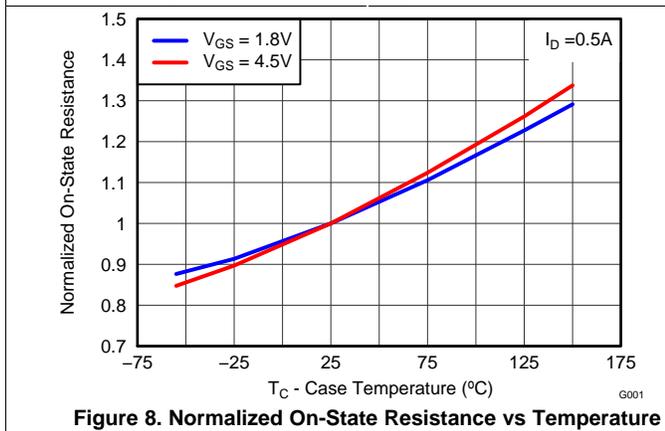
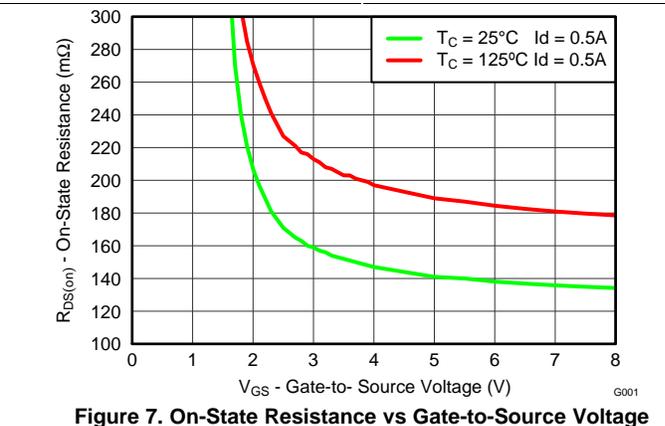
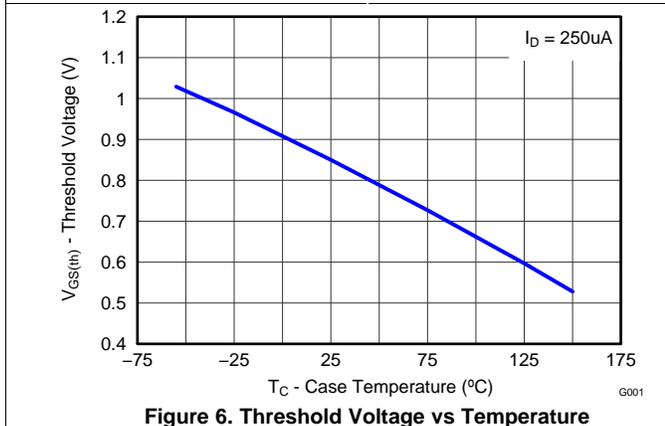
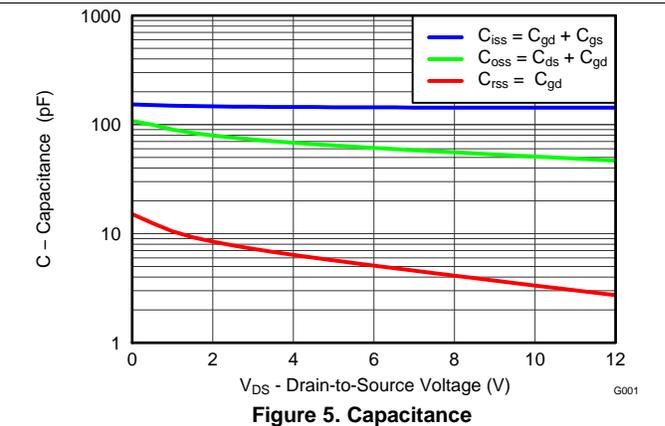
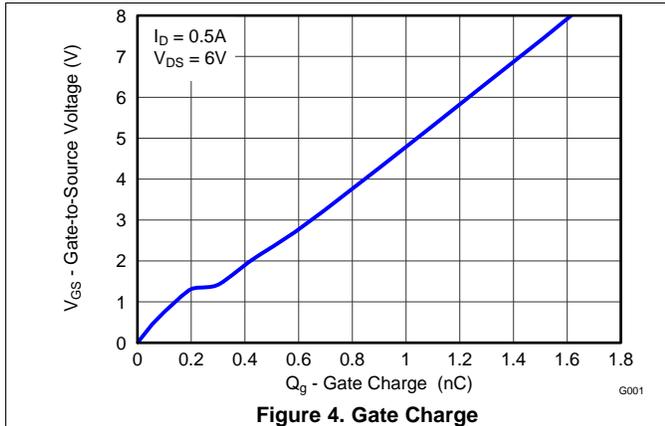
5 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

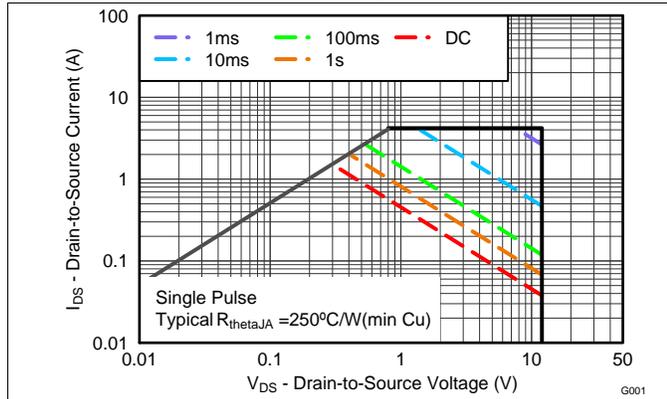


Figure 10. Maximum Safe Operating Area

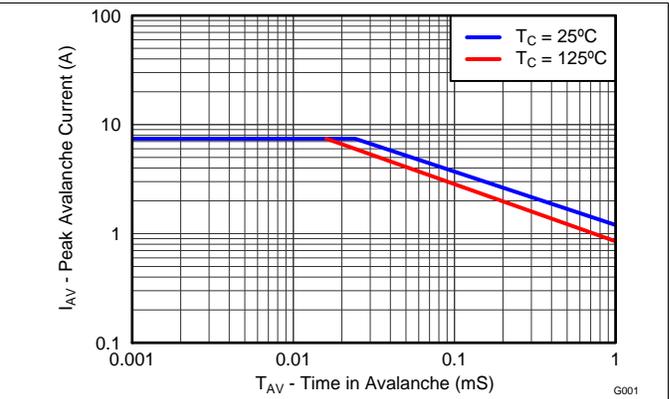


Figure 11. Single Pulse Unclamped Inductive Switching

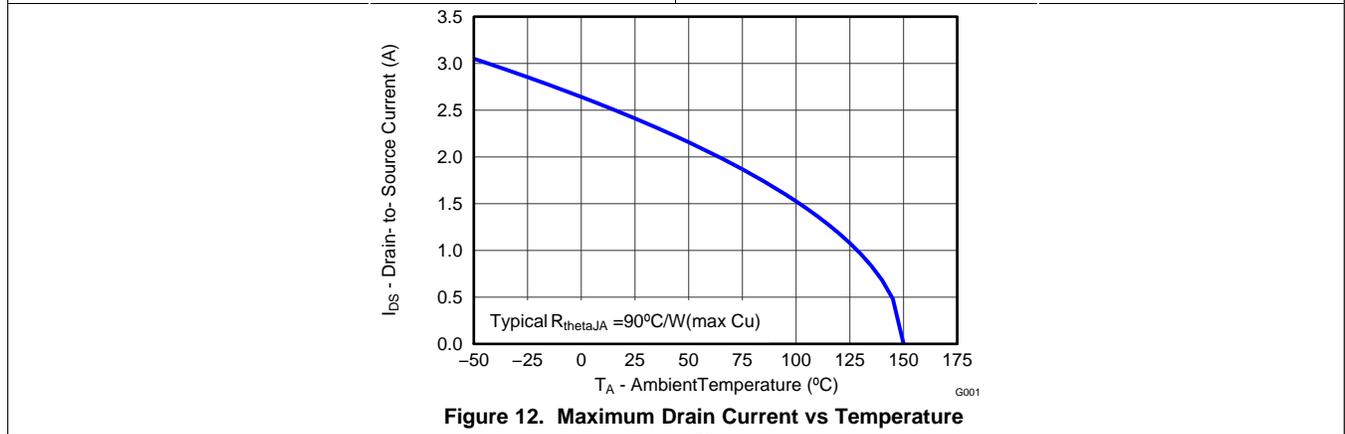
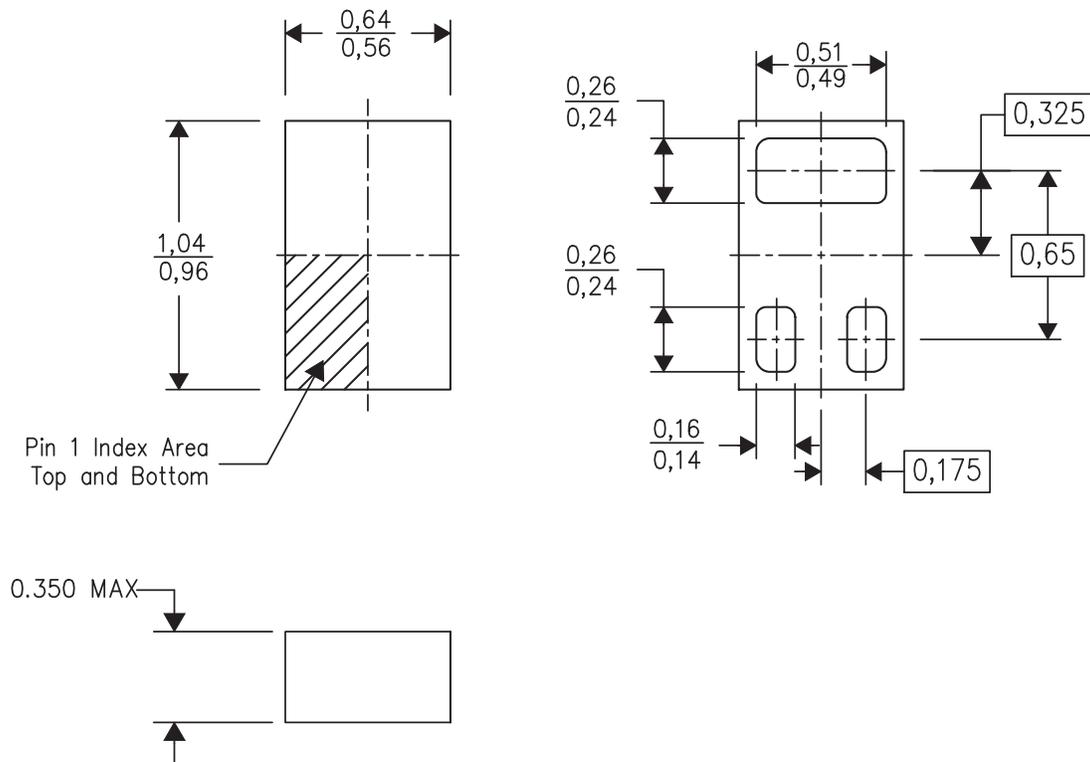


Figure 12. Maximum Drain Current vs Temperature

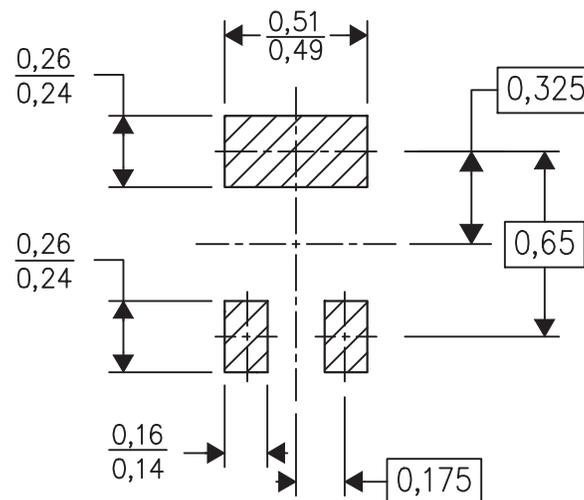
6 Mechanical Data

6.1 0402 Mechanical Dimensions



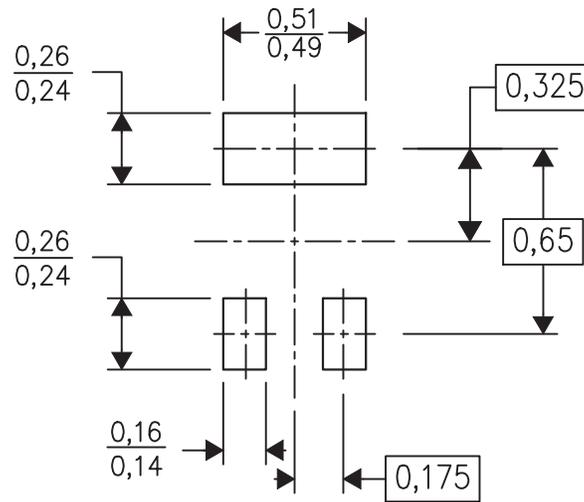
- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

6.2 Recommended Minimum PCB Layout



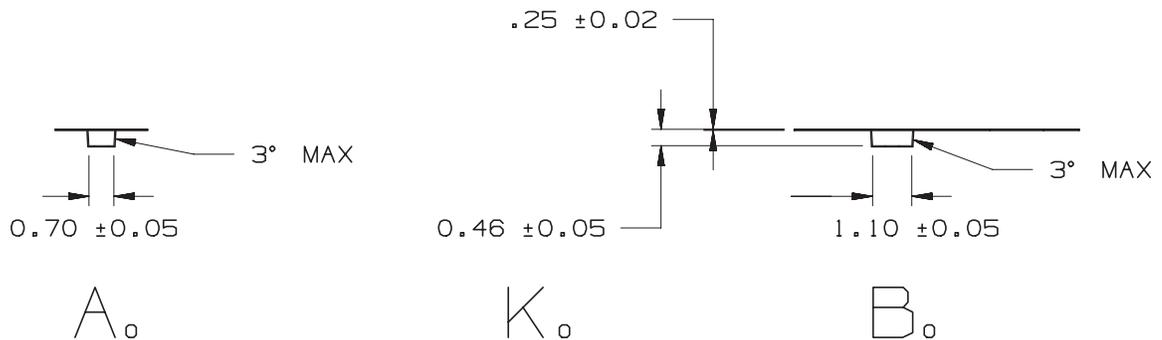
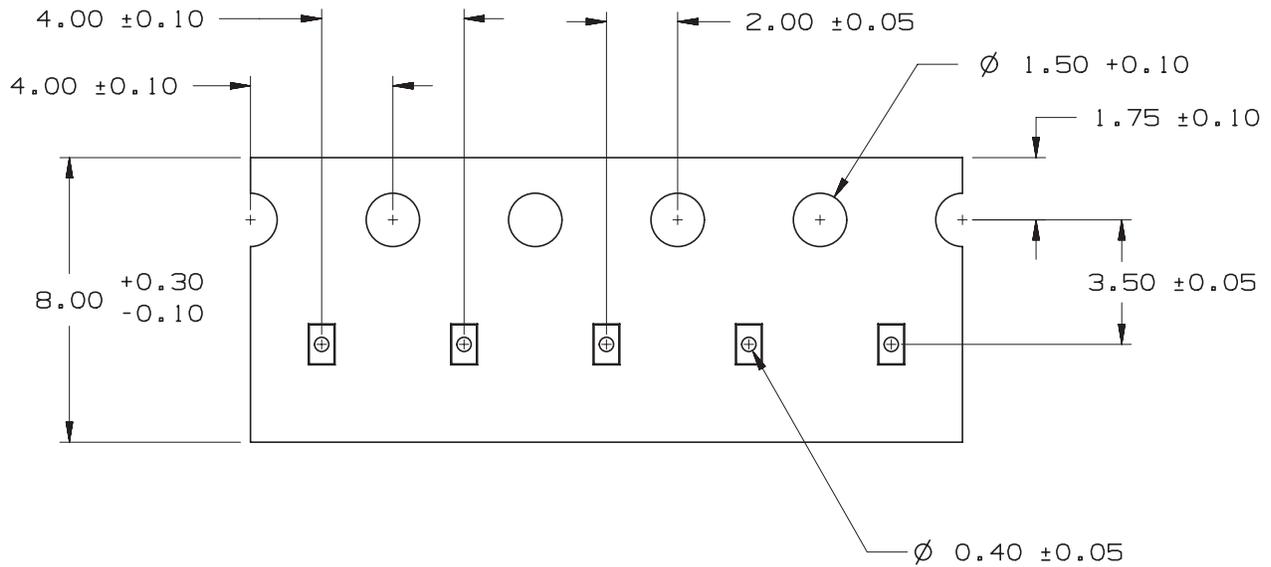
- (1) All dimensions are in millimeters.

6.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

6.4 CSD13381F4 Embossed Carrier Tape Dimensions



- (1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

7 Trademarks

FemtoFET is a trademark of Texas Instruments.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2013) to Revision B	Page
• Added I_G parameter	1
• Lowered I_{DSS} limit	2
• Lowered I_{GSS} limit	2

Changes from Original (July 2013) to Revision A	Page
• Updated title	1
• Updated device ordering information	1
• Changed test voltage conditions	2
• Changed Figure 4 Gate Charge graph	4

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